CMOS Digital Integrated Circuits: A First Course

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Edison, NJ
scitechpub.com
## CONTENTS

**Preface** xiii

**Introduction** xix
- Transistors and Computers—Until Death Do They Part xx
- Transistors and Computers—How Deep Can the Friendship Go? xxi
- Computers—Is There a Limit? xxiii
- Future xxiv

### 1 Basic Logic Gate and Circuit Theory 1

1.1 Logic Gates and Boolean Algebra 1
1.2 Boolean and Logic Gate Reduction 5
1.3 Sequential Circuits 7
1.4 Voltage and Current Laws 9
  - Terminal Resistance Analysis by Inspection 9
  - Kirchhoff’s Voltage Law and Analysis by Inspection 12
  - Kirchhoff’s Current Law and Analysis by Inspection 14
  - Mixing Voltage and Current Divider Analysis by Inspection 16
1.5 Power Loss in Resistors 18
1.6 Capacitance 21
  - Capacitor Energy and Power 22
  - Capacitive Voltage Dividers 24
1.7 Inductance 26
1.8 Diode Nonlinear Circuit Analysis 27
  - Diode Resistor Analysis 28
1.9 Some Words about Power 31
1.10 Summary 32
2 Semiconductor Physics 39

2.1 Material Fundamentals 39
  2.1.1 Metals, Insulators, and Semiconductors 39
  2.1.2 Carriers in Semiconductors: Electrons and Holes 41
  2.1.3 Determining Carrier Concentrations 43

2.2 Intrinsic and Extrinsic Semiconductors 45
  2.2.1 $n$-Type Semiconductors 45
  2.2.2 $p$-Type Semiconductors 48
  2.2.3 Carrier Concentration in $n$- and $p$-Doped Semiconductors 49

2.3 Carrier Transport in Semiconductors 51
  2.3.1 Drift Current 51
  2.3.2 Diffusion Current 52

2.4 The $pn$ Junction 56

2.5 Biasing the $pn$ Junction 59
  2.5.1 The $pn$ Junction under Forward Bias 60
  2.5.2 The $pn$ Junction under Reverse Biasing 60

2.6 Diode Junction Capacitance 62

2.7 Summary 64

3 MOSFET Transistors 67

3.1 Principles of Operation 67
  3.1.1 The MOSFET as a Digital Switch 68
  3.1.2 Physical Structure of MOSFETs 69
  3.1.3 MOS Transistor Operation: a Descriptive Approach 70

3.2 MOSFET Input Characteristics 73

3.3 $n$MOS Transistor Output Characteristics and Circuit Analysis 74

3.4 $p$MOS Transistor Output Characteristics and Circuit Analysis 83

3.5 MOSFET with Source and Drain Resistors 89

3.6 Threshold Voltage in MOS Transistors 90

3.7 Summary 93

4 Metal Interconnection Properties 99

4.1 Metal Interconnect Resistance 100
  4.1.1 Resistance and Thermal Effects 103
  4.1.2 Sheet Resistance 104
  4.1.3 Via Resistance 106
Contents

4.2 Capacitance 110
  4.2.1 Parallel Plate Model 110
  4.2.2 Capacitive Power 112
4.3 Inductance 113
  4.3.1 Inductive Voltage 113
  4.3.2 Line Inductance 115
  4.3.3 Inductive Power 116
4.4 Interconnect RC Models 117
  4.4.1 C-model for Short Lines 117
  4.4.2 RC Model for Long Lines 119
4.5 Summary 122

5 The CMOS Inverter 125
  5.1 The CMOS Inverter 125
  5.2 Voltage Transfer Curve 127
  5.3 Noise Margins 129
  5.4 Symmetrical Voltage Transfer Curve (VTC) 131
  5.5 Current Transfer Curve 132
  5.6 Graphical Analysis of VTC 134
    5.6.1 Static Transfer Curves 134
    5.6.2 Dynamic Transfer Curves 138
  5.7 Inverter Transition Speed Model 140
  5.8 CMOS Inverter Power 143
    5.8.1 Transient Power 143
    5.8.2 Short-Circuit Power 145
    5.8.3 Quiescent Leakage Power 147
  5.9 Power and Power Supply Scaling 147
  5.10 Sizing Inverter Buffers to Drive Large Loads 150
  5.11 Summary 152

6 CMOS NAND, NOR, and Transmission Gates 157
  6.1 NAND Gates 157
    6.1.1 Electronic Operation 158
    6.1.2 NAND Noncontrolling Logic State 159
  6.2 NAND Gate Transistor Sizing 162
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.3</td>
<td>NOR Gates</td>
<td>164</td>
</tr>
<tr>
<td>6.3.1</td>
<td>Electronic Operation</td>
<td>164</td>
</tr>
<tr>
<td>6.3.2</td>
<td>NOR Noncontrolling Logic State</td>
<td>165</td>
</tr>
<tr>
<td>6.4</td>
<td>NOR Gate Transistor Sizing</td>
<td>168</td>
</tr>
<tr>
<td>6.5</td>
<td>Pass Gates and CMOS Transmission Gates</td>
<td>173</td>
</tr>
<tr>
<td>6.5.1</td>
<td>Pass Gates</td>
<td>173</td>
</tr>
<tr>
<td>6.5.2</td>
<td>CMOS Transmission Gates</td>
<td>175</td>
</tr>
<tr>
<td>6.5.3</td>
<td>Tristate Logic Gates</td>
<td>176</td>
</tr>
<tr>
<td>6.6</td>
<td>Summary</td>
<td>177</td>
</tr>
<tr>
<td>7</td>
<td>CMOS Circuit Design Styles</td>
<td>185</td>
</tr>
<tr>
<td>7.1</td>
<td>Boolean Algebra to Transistor Schematic Transformation</td>
<td>185</td>
</tr>
<tr>
<td>7.2</td>
<td>Synthesis of DeMorgan Circuits</td>
<td>190</td>
</tr>
<tr>
<td>7.3</td>
<td>Dynamic CMOS Logic</td>
<td>194</td>
</tr>
<tr>
<td>7.3.1</td>
<td>Dynamic CMOS Logic Properties</td>
<td>194</td>
</tr>
<tr>
<td>7.3.2</td>
<td>Charge Sharing in Dynamic Circuits</td>
<td>196</td>
</tr>
<tr>
<td>7.4</td>
<td>Domino CMOS Logic</td>
<td>199</td>
</tr>
<tr>
<td>7.5</td>
<td>NORA CMOS Logic</td>
<td>202</td>
</tr>
<tr>
<td>7.6</td>
<td>Pass Transistor Logic</td>
<td>203</td>
</tr>
<tr>
<td>7.7</td>
<td>CMOS Transmission Gate Logic Design</td>
<td>205</td>
</tr>
<tr>
<td>7.8</td>
<td>Power and Activity Coefficient</td>
<td>206</td>
</tr>
<tr>
<td>7.9</td>
<td>Summary</td>
<td>211</td>
</tr>
<tr>
<td>8</td>
<td>Sequential Logic Gate Design and Timing</td>
<td>219</td>
</tr>
<tr>
<td>8.1</td>
<td>CMOS Latches</td>
<td>221</td>
</tr>
<tr>
<td>8.1.1</td>
<td>Clocked Latch</td>
<td>221</td>
</tr>
<tr>
<td>8.1.2</td>
<td>Gated Latches</td>
<td>222</td>
</tr>
<tr>
<td>8.2</td>
<td>Edge-Triggered Storage Element</td>
<td>223</td>
</tr>
<tr>
<td>8.2.1</td>
<td>The D-FF</td>
<td>224</td>
</tr>
<tr>
<td>8.2.2</td>
<td>Clock Logic States</td>
<td>225</td>
</tr>
<tr>
<td>8.2.3</td>
<td>A Tristate D-FF Design</td>
<td>226</td>
</tr>
<tr>
<td>8.3</td>
<td>Timing Rules for Edge-Triggered Flip-Flops</td>
<td>228</td>
</tr>
<tr>
<td>8.3.1</td>
<td>Timing Measurements</td>
<td>228</td>
</tr>
<tr>
<td>8.3.2</td>
<td>Timing Rule Violation Effect</td>
<td>230</td>
</tr>
</tbody>
</table>
## Contents

8.4 Application of D-FFs in ICs 231  
8.5 $t_{su}$ and $t_{hold}$ with Delay Elements 232  
8.6 Edge-Triggered Flip-Flop with Set and Reset 235  
8.7 Clock Generation Circuitry 236  
8.7.1 Phase Locked Loop Circuit 237  
8.8 Metal Interconnect Parasitic Effects 241  
8.9 Timing Skew and Jitter 241  
8.10 Overall System Timing in Chip Designs 242  
8.10.1 Period Constraint 243  
8.10.2 Period Constraint and Skew 244  
8.10.3 Hold Time Constraint 245  
8.10.4 Period Constraint with Skew and Jitter 246  
8.11 Timing and Environmental Noise 249  
8.12 Summary 251  

9 IC Memory Circuits 261  
9.1 Memory Circuit Organization 262  
9.2 Memory Cell 264  
9.3 Memory Decoders 266  
9.3.1 Row Decoders 266  
9.3.2 Column Decoders 267  
9.4 The Read Operation 269  
9.5 Sizing Transistor Width to Length Ratio for Read Operation 270  
9.6 Memory Write Operation 272  
9.6.1 Cell Write Operation 272  
9.6.2 Latch Transfer Curve 273  
9.7 Sizing Transistor Width to Length Ratio for Write Operation 273  
9.8 Column Write Circuits 277  
9.9 Read Operation and Sense Amplifier 278  
9.10 Dynamic Memories 281  
9.10.1 3-Transistor DRAM Cell 283  
9.10.2 1-Transistor DRAM Cell 284  
9.11 Summary 285
10 Programmable Logic—FPGAs

10.1 A Simple Programmable Circuit—The PLA
10.1.1 Programmable Logic Gates
10.1.2 AND/OR Matrix Gates

10.2 The Next Step: Implementing Sequential Circuits—The CPLDs
10.2.1 Incorporating Sequential Blocks—The Complex Programmable Logic Device (CPLD)
10.2.2 Advanced CPLDs

10.3 Advanced Programmable Logic Circuits—The FPGA
10.3.1 Actel ACT FGPAs
10.3.2 Xilinx Spartan FGPAs
10.3.3 Altera Cyclone III FGPAs
10.3.4 Today’s FPGAs
10.3.5 Working with FPGAs—Design Tools

10.4 Understanding the Programmable Technology
10.4.1 Antifuse Technology
10.4.2 EEPROM Technology
10.4.3 Static RAM Switch Technology

11 CMOS Circuit Layout

11.1 Layout and Design Rules
11.2 Layout Approach: Boolean Equations, Transistor Schematic, and Stick Diagrams
11.3 Laying out a Circuit with PowerPoint
11.4 Design Rules and Minimum Layout Spacing
11.5 Laying out a CMOS Inverter
11.5.1 pMOS Transistor Layout
11.5.2 Revisiting the Design Rules of the pMOS Transistor Layout
11.5.3 nMOS Transistor Layout
11.5.4 Merging Transistors to a Common Polygate
11.6 Completed CMOS Inverter Drawn to Design Rule Minimum Dimensions
11.7 Multi-Input Logic Gate Layouts
11.8 Merging Logic Gate Standard Cell Layouts
11.9 More on Layout
## Contents

11.10 Layout CAD Tools
11.11 Summary

12 How Chips Are Made

12.1 IC Fabrication Overview
12.2 Wafer Construction
12.3 Front and Back End of Line Fabrication
12.4 FOL Fab Techniques
  12.4.1 Oxidation of Silicon
  12.4.2 Photolithography
  12.4.3 Etching
  12.4.4 Deposition and Implantation
12.5 Cleaning and Safety Operations
12.6 Transistor Fabrication
12.7 Back End of Line BOL Fab Techniques
  12.7.1 Sputtering
  12.7.2 Dual Damascene
  12.7.3 Interlevel Dielectric and Final Passivation
12.8 Fabricating a CMOS Inverter
  12.8.1 Front End of Line Operation
  12.8.2 Back End of Line Operation
12.9 Die Packaging
12.10 IC Testing
12.11 Summary

Answers to all Even Numbered end of Chapter Exercises
Index
This book teaches introductory complementary metal-oxide-semiconductor (CMOS) digital electronics for electrical and computer engineering undergraduates. For many years the CMOS technology has dominated the method of designing and manufacturing digital (computing) integrated circuits. The selection of material here is not significantly different from the graduate texts by J. Rabaey et al. (Digital Integrated Circuits, 2003, Prentice Hall), N. Weste and D. Harris (CMOS VLSI Design, 2011, Addison-Wesley), or J. Baker (CMOS: Circuit Design, Layout, and Simulation, 2010, Wiley-IEEE Press), but the style is introductory with many examples, self-exercises, and end-of-chapter problems.

This book initially reviews material relevant to digital electronics that students learned in previous circuit and logic courses. The book then moves through chapters on basic physics of semiconductor materials and diodes; nMOS and pMOS field effect transistors circuit analysis; electronic properties of the metal interconnections; the CMOS inverter; the CMOS NAND, NOR, and transmission gates electronics; transformation from Boolean equations to CMOS transistor schematics and domino circuits; timing electronics; memory circuits; field-programmable gate arrays (FPGAs); CMOS layout; and CMOS fabrication basics. The emphasis is on transistor level electronics.

The principles of power dissipation are introduced with numerical examples. Lowering circuit power has special urgency today where total Internet power consumes about 10% of US electrical power generation.

Other features and objectives include:

- There are abundant examples, self-exercises with answers, and many problems at the end of chapters to give students reflexive skills in transistor circuit analysis.
- This course can be taught before or after a companion class in introductory analog electronics.
- The book strives for clarity and self-learning in an undergraduate presentation.
- The book doesn’t overwhelm students with too much details; it defines teaching goals consistent with what they will take forward to the next level of electronics.
- Students are provided with an education that serves as a prerequisite for graduate or senior courses in digital electronics and allows entry level into the digital electronics industry.
- The book is light enough for students to carry to class.
Chapter Summaries

Chapter 1 reviews relevant logic theory that includes Boolean equation to logic gate schematics, DeMorgan’s theorem, logic equivalence, and logic gate reduction. Basic circuit theory is next, with emphasis on analysis of terminal impedance, node voltages, and branch currents by inspection. Nonlinear circuit analysis techniques are introduced using the diode and its nonlinear current-voltage expression. Capacitor and inductor properties and circuits are reviewed, as is the power wasted in resistive and capacitive circuits. These topics are a few among many but are selected for their relevance in the digital circuit analysis that follows.

The second chapter introduces the semiconductor physics that underlie device operation. The goal is to impart a good visual model of the physics of materials and diodes, and to use basic equations for better understanding. Semiconductor physics is a complex subject that can involve more than one course at the graduate level, and Chapter 2 cannot replicate this. However, visual models of semiconductor materials and diodes are important because engineers often use qualitative language to communicate important properties of the physics of semiconductor diodes and transistors. Students should be able to answer the question, “How do diodes (and transistors) work and perform basic parameter calculations?” This chapter leads directly into Chapter 3 on field effect transistors.

CMOS circuits use two transistor types; the nMOS and pMOS field effect transistors. Chapter 3 describes how these transistors work, followed by numerical analysis of circuit node voltages and currents. Many examples, self-exercises, and end-of-chapter problems give students the reflexive response to analyze transistor digital circuits. Equal treatment is given to each transistor type.

Chapter 4 deals with metal properties, which are especially relevant in modern circuits since chip total metal length may be on the order of several miles, and minimum metal dimensions can be 22 nm or smaller. Metal properties are a major concern in attaining maximum IC frequency and minimum noise operation, and metal physics deserves as much study as does the transistor.

In Chapter 5, the CMOS inverter is discussed. The CMOS inverter is the most abundant logic gate in any digital integrated circuit (IC). It has one nMOS and one pMOS field effect transistor. This chapter introduces about a dozen important electronic properties, with numerical examples. Inverter properties are inherently important but are also the basis for electronic properties of NAND, NOR, and sequential logic circuits such as the master-slave flip-flop. Inverter power dissipation properties are emphasized.

Chapter 6 covers NAND and NOR gates, which build on the inverter by placing transistors in parallel and series to the inverter pair. These multi-input logic gates have all of the electronic properties of the inverter and a few that are unique. The electronic basis for the noncontrolling logic state is described in this chapter as it relates to circuit debugging, test engineering, and schematic reading. Pass transistor and CMOS transmission gate properties conclude the chapter. Transmission gates are abundant, comprising half of the logic gates in the master-slave flip-flop.
Chapter 7 develops design styles that assemble transistors into logic gates. It begins with a relatively simple technique to transform Boolean equations into a CMOS transistor schematic that performs the logic. Other design styles are presented along with the reasons for having different styles. Power dissipation is analyzed with a technique that allows a power comparison of different combinational logic configurations.

Chapter 8 discusses the accurate design and placement of timing signals, which may be the most challenging task for a designer. This often neglected undergraduate course topic is emphasized, giving it the importance it deserves. The edge-triggered flip-flop (FF) has a complexity that must be mastered. Timing parameters and rules must be exact otherwise circuits will fail. System-level timing builds on these foundations and introduces system timing parameters and constraints.

Chapter 9 covers memory circuits. They have always been embedded within the computing chips, but today microprocessor chips may dedicate more than 70% of the total transistor count to these memory circuits. Therefore, special emphasis is given on these static random access memory (SRAM) designs. Transistor sizing of SRAM cells is developed with numerical examples. Another high-volume memory design is dynamic random access memory (DRAM). This single transistor memory cell has different properties.

Chapter 10 looks at a unique and popular design style using field-programmable gate arrays (FPGA). This material follows from other design styles described in the preceding chapter. The electronics and method of operation are different, but FPGAs are common and abundant enough to devote a chapter.

In Chapter 11, the CMOS layout is discussed. A conversion occurs in the design process when transistor schematics are transformed to rectangular images on a photographic mask. The images represent transistor and metal line geometries. Masks are drawn for each of several layers in the buildup of the IC. Layout is not electronics but is the necessary first step in using photolithography to make the tiny transistors and metal interconnections. The mask layout step is introduced using manual layout of the inverter, NAND, and NOR gates. Several commercial layout tools exist, but cost and training time led us to consider the Microsoft PowerPoint program to draw the layouts. PowerPoint is typically available on all computers, training time is minimal, it appears to have long-term stability in the market, and students get a better grounding in design rules. PowerPoint has been successful as a teaching tool in the classroom for layout of simple logic gates circuits.

Chapter 12 describes the chemical, physical, and photolithography techniques that actually make the final circuit. This chapter is qualitative but sufficient enough to allow students to converse on the various sequenced fabrication techniques that achieve the end circuit result of the chip.

Comments for Instructors

The book uses long channel models for MOSFET analysis, even though short channel models are common in industry. The reasons are twofold. First, the short channel models are often simplified for undergraduate presentation where they lose accuracy. Also,
full short channel models become too complex for hand calculations. Although the long channel models are also not accurate, they allow manual problem solving insight into the various bias regions of the transistors. We originally designed the book using short channel models, but found the simplified analytical expressions clumsy and inaccurate. A second observation is that modern industry electronic papers and oral presentations often refer to long channel models despite the use of short channel transistors. It is part of the language. The more accurate short channel models are best left to graduate courses and detailed computer models.

Other choices were made to avoid overly complex material at this undergraduate stage. The subjects and their depth were a trade-off between designing a one-term course and covering the important topics. For example, combinational logic power analysis uses the truth table analysis rather than logical effort. Chapter 9 on memory keeps the timing description simple but to the point. Memory design deserves a whole book for a full description.

The problems in this book most efficiently use the modern equation solving ability of scientific calculators. One great learning advantage is that time is spent on the problem itself and little on the grind of manually solving with quadratic equations or iteration. An unknown variable can be embedded anywhere in the equation, and the scientific calculator doesn’t care. It solves for the unknown variable in seconds. Students and instructors can solve these problems any way they desire, but the scientific calculator is truly an advance in modern digital circuit teaching.

A Suggested Semester Chapter Order

<table>
<thead>
<tr>
<th>CHAPTER</th>
<th>TITLE</th>
<th>TIME IN CLASS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chapter 1</td>
<td>Basic Logic Gates and Circuit Theory</td>
<td>1 week</td>
</tr>
<tr>
<td>Chapter 2</td>
<td>Semiconductor Physics</td>
<td>1 week</td>
</tr>
<tr>
<td>Chapter 3</td>
<td>MOSFET Transistors</td>
<td>2 weeks</td>
</tr>
<tr>
<td>Chapter 5</td>
<td>CMOS Inverter</td>
<td>1.5 weeks</td>
</tr>
<tr>
<td>Chapter 6</td>
<td>CMOS NAND, NOR, and Transmission Gates</td>
<td>1 week</td>
</tr>
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<td>Chapter 7</td>
<td>CMOS Design Styles</td>
<td>1.5 weeks</td>
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<tr>
<td>Chapter 11</td>
<td>CMOS Circuit Layout</td>
<td>1 week</td>
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<tr>
<td>Chapter 12</td>
<td>How Chips are Made</td>
<td>1 week</td>
</tr>
<tr>
<td>Chapter 4</td>
<td>Metal Interconnection Properties</td>
<td>1 week</td>
</tr>
<tr>
<td>Chapter 8</td>
<td>Sequential Logic Gate Design and Timing</td>
<td>2 weeks</td>
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<tr>
<td>Chapter 9</td>
<td>Memory Circuits</td>
<td>1 week</td>
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<tr>
<td>Chapter 10</td>
<td>FPGAs</td>
<td>0.5 week</td>
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</tbody>
</table>

Chapter 4 on metal interconnects logically fits with device descriptions, but it interrupts the flow of electronic circuitry so it was put later. Chapters 11 and 12 continue the emphasis on circuitry and the IC before returning to Chapter 4.
Author Background

This book reflects the experience of the authors, who have taught this material at the graduate and undergraduate level and have worked closely with the digital electronic industry in their careers. Hawkins and Segura did sabbaticals with the Intel Corporation: Segura at the Intel campus in Portland Oregon, and Hawkins in Rio Rancho, New Mexico. Segura also did sabbatical work at Philips Semiconductor and received numerous research contracts from industry. Hawkins worked closely with the Sandia National Laboratory in New Mexico for over 20 years in its CMOS integrated circuits group. Both authors have long histories of committee work for the European DATE conference, the International Test Conference, and the VLSI Test Symposium. Hawkins was editor of the Electron Device Failure Analysis magazine.

Payman Zarkesh-Ha is professor in the ECE Department at the University of New Mexico (UNM). He teaches graduate and undergraduate VLSI, digital, and analog electronics. Prior to joining UNM, he worked for five years at LSI Logic Corp, where he worked on interconnect architecture design for the next ASIC generations. He has published more than 60 refereed papers and holds 12 issued patents. His research interests are statistical modeling of nanoelectronics devices and systems, and design for manufacturability, low power, and high performance VLSI designs. All of these activities outside of the classroom influenced our choice of material and style in the book. It is long overdue for electrical and computer engineering undergraduate students to rid themselves of outdated logic circuits and receive a course dedicated to digital CMOS electronics.